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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,825	09/25/2003	Maximino Aguilar JR.	AUS920030704US1	7315

50170 7590 04/05/2007  
IBM CORP. (WIP)  
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EXAMINER
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PARTHASARATHY, PRAMILA

ART UNIT	PAPER NUMBER
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2136

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No. 10/670,825	Applicant(s) AGUILAR ET AL.	
	Examiner Pramila Parthasarathy	Art Unit 2136	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>9/2003; 69, 11/2005; 7, 8/2006</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This action is in response to the communication 09/28/2006. Preliminary amendments to the claims were filed. New claims 31 – 33 were added. Claims 1 – 33 are currently pending.

### ***Inventorship***

2. In view of the papers filed on 7/13/2006, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by addition of the following two inventor names: Akiyuki Hatakeyamma and Masakazu Suzuoki.

The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of Office records to reflect the inventorship as corrected.

### ***Information Disclosure Statement***

3. Initialed copies of IDS that were filed on September 25, 2003, June 07, 2005, November 11, 2005, July 25, 2005 and August 18, 2006 are attached to this office action.

***Claim Objections***

4. Claim 1 is objected to because of the following informalities: Claim 1 recites, "...an encryption process corresponding to the request" and "...sending an encryption request from a first processor in the at least one first processor to the second processor". Replace "an encryption process corresponding to the request" and "...sending an encryption request from a first processor in the at least one first processor to the second processor" with "an encryption process corresponding to the **encryption** request" and "...sending an encryption request from the first processor to the second processor". (Emphasis added).

Claims 8, 18 and 28 are objected to because of the following informalities:  
Claims 8, 18 and 28 recite, "DMA". Expand the acronym "**DMA**". (Emphasis added).

Claim 31 is objected to because of the following informalities: Claim 31 recites, "multiprocessor system to be in an shared operation state" and "the at least one second processor". Replace "an shared" with "a shared" and "**the second processor**". (Emphasis added).

Appropriate corrections are required.

***Claim Rejections - 35 USC § 101***

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1 – 33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim(s) 31 – 33 are not limited to tangible embodiments as they recite “configuring” and “executing” functions, which do not define any structural and functional interrelationships between the method, program or instructions and other claimed aspects of the invention, which permits the program’s functionality to be realized.

The rejection of the base claim is necessarily incorporated into the dependent claims.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 – 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 31, 32 and 33 recite "the first processor executes the first code in a secure manner by virtue of the isolated operational state". However, Claims 31, 32 and 33 also recite "at least one first processor of the multiprocessor system to be in a shared operational state, wherein the shared operation state causes the at least one first processor to operate using a common memory accessible by a plurality of processors in the multiprocessor system" and "a second processor of the multiprocessor system to be in an isolated operational state". The rejection of the base claim is necessarily incorporated into the dependent claims.

Examiner interprets that the first and second processors execute all code in a shared (unsecured) operational state using common memory accessible by a plurality of processors in the multiprocessor system.

Claims 10, 20 and 30 recite "the encryption process is selected from the group consisting of a decryption function, an encryption function, and an authentication function". However, Claims 1, 11 and 21 recite "the encryption process being effective to or adapted to transform the data".

Examiner is unclear how "an authentication function" transforms the data. Examiner interprets that the encryption process (being effective to or adapted to transform the data), is selected by an authentication function.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 – 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Sibert (U.S. Patent Number 7,124,170).

8. As per Claims 31 – 33, Sibert teaches “configuring at least one first processor of the multiprocessor system to be in a shared operational state, wherein the shared operation state causes the at least one first processor to operate using a common memory accessible by a plurality of processors in the multiprocessor system (Column 9 lines 15 – 60, processor runs in non-critical or non-privileged mode);

configuring a second processor of the multiprocessor system to be in an isolated operational state, wherein the isolated operational state causes a local memory associated with the first processor to be not accessible by the at least one first processor (Column 6 lines 43 – 56, Column 9 lines 15 – 60 and Column 10 lines 14 – 21, processor runs in critical and privileged mode);

executing first code within the first processor in a secure manner by virtue of the isolated operation operational state (Column 10 lines 23 – 46); and

executing second code within the at least one second processor in an unsecured manner by virtue of the shared operational state (Column 10 lines 23 – 46, write access to memory region succeeds).

9. As per Claims 1, 11 and 21, Sibert teaches "sending an encryption request from a first processor in the at least one first processor to the second processor" (Column 17 lines 23 – 48);

receiving, at the second processor, an encryption request (Column 17 lines 23 – 48);

reading data from the common memory into the local memory associated with the second processor, wherein the reading is performed by the second processor (Column 17 lines 23 – 48);

executing at the second processor, an encryption process corresponding the request, the encryption process being adapted to transform the data (Column 17 lines 23 – 48); and writing the transformed data from the second processor to the common memory (Column 17 lines 23 – 51, process stores the encrypted result (transformed data) in secure internal memory and/or in insecure external (common) memory).



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**10.** As per Claim 2, 12 and 22, Sibert teaches "reading, at the second processor, one or more special nonvolatile registers, the special registers including one or more encryption keys"(Column 16 lines 41 – 59 and Column 17 lines 40 – 48);

"using one or more of the encryption keys in the encryption process" (Column 16 lines 41 – 59 and Column 17 lines 23 – 48).

**11.** As per Claim 3, 13 and 23, Sibert teaches "the sending further comprises the request to a mailbox that corresponds to the second processor and the receiving further comprises checking the second processor's mailbox from the second processor" (Column 17 lines 23 – 48, security registers (mailbox) corresponding to the second processor indicates whether they have been tampered or not).

**12.** As per Claim 4, 14 and 24, Sibert teaches "identifying an input data area in the common memory from which the data is read and an output buffer area into which the transformed data is written"(Column 17 lines 40 – 51).

**13.** As per Claim 5, 15 and 25, Sibert teaches "reading, from the common memory, initialization software code to be executed on the second processor; and authenticating the initialization software code" (Column 15 line 66 – Column 16 line 25 and Column 17 lines 23 – 48);

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**14.** As per Claim 6, 16 and 26, Sibert teaches “the authenticating is performed by a routing stored in a nonvolatile memory and wherein the executing of the encryption process is only performed if the initialization software code is successfully authenticated” (Column 21 lines 38 – 65 and Column 22 lines 8 – 26).

**15.** As per Claim 7, 17 and 27, Sibert teaches “reading, at the second processor, one or more special nonvolatile registers, the special nonvolatile registers including one or more encryption keys, after the initialization software code is successfully authenticated; and restricting access to the special nonvolatile registers from outside of the second processor” (Column 20 lines 43 – 58).

**16.** As per Claim 8 and 28, Sibert teaches “the reading and writing steps are performed using DMA operations” (Column 6 lines 43 – 56).

**17.** As per Claim 18, Sibert teaches “a DMA controller associated with each of the plurality of processors, wherein the second processor reads from and writes to the common memory using DMA operations performed by the second processor’s DMA controller” (Column 6 lines 43 – 56).

**18.** As per Claim 9, 19 and 29, Sibert teaches “identifying the encryption process and an encryption algorithm from a plurality of encryption process and encryption algorithms based upon the encryption request” (Column 17 lines 23 – 48 and Column 20 lines 19 – 67);

“loading encryption software code corresponding to the identified encryption process and the encryption algorithm, the loading being performed by reading the encryption software code from the common memory to the second processor’s local memory” (Column 17 lines 23 – 48 and Column 20 lines 19 – 67).

**19.** As per Claim 10, 20 and 30, Sibert teaches “the encryption process is selected from the group consisting of a decryption function, an encryption function, and an authentication function” (Column 20 lines 19 – 67).

### ***Conclusion***

**20.** Examiner’s Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

**21.** The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO Form 892.

Applicant is urged to consider the references. However, the references should be evaluated by what they suggest to one versed in the art, rather than by their specific disclosure. If applicants are aware of any better prior art than those are cited, they are required to bring the prior art to the attention of the examiner.

**22.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pramila Parthasarathy whose telephone number is 571-272-3866. The examiner can normally be reached on 8:00a.m. To 5:00p.m.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-232-4195. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR only. For more information about the PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pramila Parthasarathy  
April 01, 2007.

A handwritten signature in black ink, appearing to be 'Pramila Parthasarathy', written over a horizontal line.